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DESIGN OF CMOS QUADRATURE VCO USING ON-CHIP TRANS-DIRECTIONAL COUPLERS

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Abstract—This work presents a quadrature voltage-controlled oscillator (QVCO) realized by on-chip trans-directional (TRD) couplers. The TRD coupler is implemented by sections of parallel-coupled lines connected by shunt capacitors periodically. The TRD couplers allow decoupling the DC path between input and output. Thus, it can make connections with active circuits easier, eliminating some off-chip biasing circuits. Since the quadrature signals are generated by 90° hybrid couplers, the oscillator core can be optimized for circuit performance without considering the generation of quadrature signals. A Ka band QVCO fabricated in CMOS 0.18 μm technology was designed to verify the effectiveness of the proposed QVCO structure. The measurement results reveal that the quadrature output signals of QVCO have about −1.52 dBm output powers with less than 1 dB amplitude imbalance and less than 6° phase difference in the frequency range of 31.9 to 32.7 GHz. The best measured phase noise of the QVCO is −110.6 dBc/Hz at 1 MHz offset from the center frequency. The figure-of-merit of the circuit is 187.5 dBc/Hz.

1. INTRODUCTION

QVCO is a widely used component in modern digital communication systems. Wireless transceivers usually adopt the quadrature local oscillation signaling scheme to reject unwanted image signals during the up- or down-conversion of the communication signals. In published papers, the most commonly used structure is the one using two

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pairs of cross-coupled VCOs connected by parallel or series coupling transistors [1–4]. However, such a structure is difficult to operate above 20 GHz because of the device delay of the cross-coupling transistors and the parasitic effect of the interconnections inside the circuits [5–8]. Another disadvantage of this structure is that a compromise must be made among quadrature accuracy, power consumption and phase noise. Therefore, a rotary traveling-wave topology is proposed to form the multiphase VCO [9] in which phase delay lines are used, limiting its operation bandwidth. Besides, lots of CMOS VCOs or QVCOs adopt open drain buffers as output stages, leaving the separation of DC and RF path to off-chip circuits such as bias-Ts [10–12]. For a single chip solution, adding on-chip DC blocking circuits will enlarge chip sizes and deteriorate the output signals.

In [13], a novel TRD coupler implemented by parallel coupled microstrip lines is proposed as shown in Fig. 1. This coupler is constructed by sections of coupled lines with shunt capacitors placed periodically between them. Unlike codirectional and contradirectional couplers [14–16], the through and coupled ports of this TRD coupler are on the same microstrip line. Thus, it has the benefit of DC isolation between input and output ports. And it does not use the composite right/left handed structure [17–20]. When connected to active circuits, it is possible to utilize this feature to save DC blocking circuits. In [13], quadrature hybrids based on the TRD coupler have been designed and fabricated. Good quadrature phase difference and amplitude balance between the two output ports over a 26% bandwidth have been achieved in this work.

Figure 1. Topology of the proposed TRD coupler.

In this paper, we propose a novel QVCO in which two quadrature hybrids implemented by TRD couplers are connected to the output ports of a cross-coupled VCO to generate quadrature signals. Since the required quadrature phase and equal amplitude of the quadrature signals mainly depend on the performance of the quadrature hybrids, the cross-coupled VCO can be optimized to achieve lowest phase noise or maximum output power. Due to the TRD couplers, circuits for DC and RF separation can also be avoided.

To verify the characteristics of the proposed QVCO, a Ka-band prototype was designed and fabricated in CMOS 0.18-μm technology. The measured results show that the output power at each port reaches

-1.52 dBm in the frequency range of 31.9 to 32.7 GHz. The best measured phase noise is -110.6 dBc/Hz at 1 MHz offset frequency of the carrier frequency. The figure-of-merit (FOM) is 187.5 dBc/Hz which is considered high for a Ka-band QVCO.

In the following section, the analysis and design of the proposed quadrature hybrids based on the TRD couplers is presented. In Section 3, the proposed QVCO is designed and fabricated. Finally, conclusions are given in Section 4.

2. DESIGNS AND IMPLEMENT OF THE TRD COUPLER

A TRD CPW coupler as shown in Fig. 2(a) is consisted of identical sections of parallel coupled CPWs and shunt capacitors implemented by floating plates. The floating plate in each cell creates extra capacitances among itself, the coupled lines and the ground. The equivalent circuits are shown in Fig. 2(b). To increase the capacitance between the floating plates and the coupled lines, the CTM5 layer is added between the two metal layers to reduce the effective distance between them [21] (Fig. 2(c)).

According to the even- and odd- mode analysis in [13], the impedance Z_e, Z_o, and the loaded capacitor C_e, and C_s of the cells of TRD coupler, as shown in Fig. 3, can be derived as

$$Z_e = Z_0 \cdot \sqrt{\frac{1+k}{1-k}} \Big/ \sqrt{\frac{\sin(\theta/N) + (\cos(\theta/N)-1)(\cos(\theta/N) - \cos(\pi/2/N))/\sin(\theta/N)}{\sin(\theta/N) + (\cos(\theta/N)+1)(\cos(\theta/N) - \cos(\pi/2/N))/\sin(\theta/N)}} \quad (1)$$

$$Z_o = Z_0 \cdot \sqrt{\frac{1-k}{1+k}} \Big/ \sqrt{\frac{\sin(\theta/N) + (\cos(\theta/N)-1)(\cos(\theta/N) - \cos(3\pi/2N))/\sin(\theta/N)}{\sin(\theta/N) + (\cos(\theta/N)+1)(\cos(\theta/N) - \cos(3\pi/2N))/\sin(\theta/N)}} \quad (2)$$

$$C_e = 2(\cos(\theta/N) - \cos(\pi/2N))/(2\pi f Z_e \sin(\theta/N)) \quad (3)$$

$$C_s = (2(\cos(\theta/N) - \cos(3\pi/2N))/(2\pi f Z_o \sin(\theta/N)) - C_e)/2, \quad (4)$$

where parameters N, k, θ and f mean the number of cells, coupling factor, electrical length of the coupled-line, and center frequency, respectively. Comparing of Fig. 2 and Fig. 3, the equivalent circuit

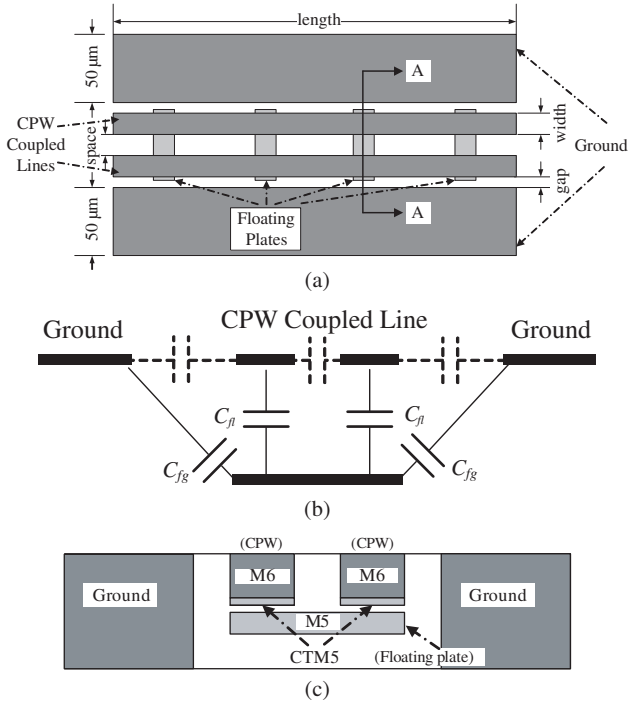

Figure 2. (a) Topology of TRD coupler in the integrated technology. (b) The equivalent capacitance network of AA cross section. (c) Layout of AA cross section.

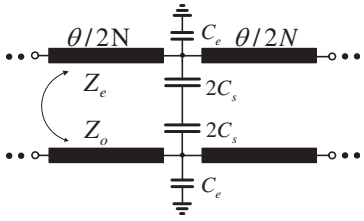

Figure 3. Equivalent circuit of periodical loaded coupled-line cell of TRD coupler.

parameters of the floating plate can be related as follows

$$C_e = \frac{1}{1/C_{fg} + 1/C_{fl}} \tag{5}$$

$$C_s = C_{fl}/2 \tag{6}$$

Table 1. Parameters of the TRD coupler.

TRD Coupler	Parameters values
Center Frequency (GHz)	30
Space (μm)	23
Width (μm)	21
Gap (μm)	12
Length (μm)	880
Number of Cells N	4
θ	66°
k	−3 dB
Z_e (Ω)	89.4
Z_o (Ω)	51.5
C_s (fF)	201.5
C_e (fF)	14.6

According to [13], the larger the number of sections adopted in the design of the TRD coupler, the wider the operation bandwidth. It also mentions that the bandwidth increase is very small when the number of cells changes from four to six or more. EM simulation also indicates that the output of the through and coupled ports will deteriorate as the number of cells becomes larger. Thus, a four-cell design is selected as a compromise between bandwidth and insertion loss.

Based on the design Equations (1)–(4) and the equivalent model, a 3-dB TRD coupler operating at 30 GHz is designed and simulated. The complete circuit is simulated by Agilent Advanced Design System (ADS) software. However, due to the minimum line width limitation of TSMC 0.18 μm CMOS process, a port impedance of 27 Ω is required to lower the even-mode characteristic impedance of the coupled line such that it can be realizable. Also, the line widths of the couplers are also limited by the current density on the metal strip, imposing a minimum line width of 13.5 μm. The circuit parameters of this coupler are listed in Table 1. The computed results according to (1)–(4) and the TRD model in Fig. 3 are presented in Fig. 4. It can be seen that the bandwidth is from 25.95 to 33.8 GHz under the criteria of 90° ± 5° phase difference and ±1 dB amplitude difference. Since the port impedance of the coupler is no longer matched to the 50 Ω measurement standard, it is expected that the measured performance will be degraded. Fig. 5 (a) shows the computed result after taking into the account of the mismatch. The isolation, return loss and coupling

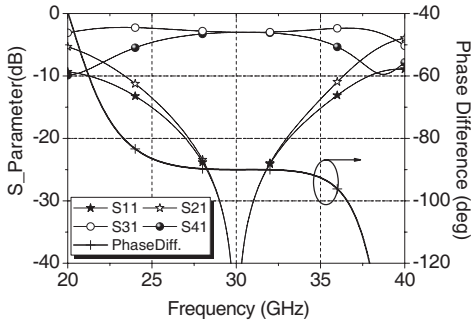

Figure 4. The computed simulation of the S-Parameters of the coupler.

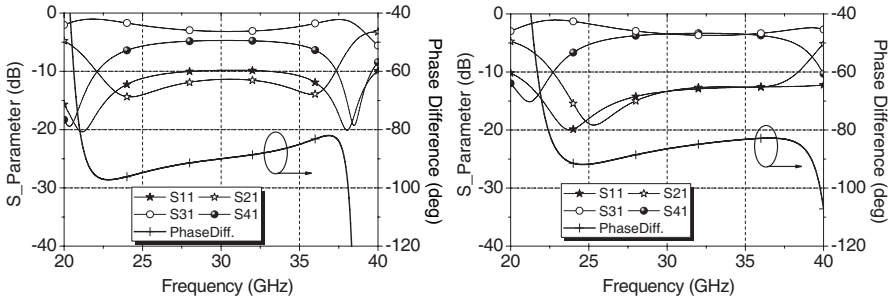

Figure 5. (a) Computed result at 50 Ω port impedance. (b) Computed result at 50 Ω port impedance after fine-tuning C_e and C_s.

factor are all degraded. To remedy this, C_e and C_s are fine-tuned from 14.6 fF to 1.2 fF and from 202 fF to 185 fF, respectively. Fig. 5(b) shows the initial computed results after this adjustment. Significant improvement in return loss and amplitude imbalance is observed at the sacrifice of phase difference as indicated in Table 2. which shows the performance comparison before and after fine-tuning the shunt capacitance.

The C_s value can be approximated by the ideal parallel plate capacitor model, while the C_e value has to be extracted from full-wave simulation. The C_e value mainly depends on the distance of the edges of the floating plates to the ground. By changing the size of the floating plate, the required C_e and C_s values can be realized. Fig. 6 shows that the extracted capacitances from the simulated results of the floating plate with a size of 26 μm × 15.5 μm match the required capacitances. The total electrical length of the proposed coupler is only 66° as a result of the added shunt capacitances.

Table 2. Comparison of the computed results at 30 GHz before and after fine-tuning of C_e and C_s.

	Before tuning C_e and C_s	After tuning C_e and C_s
Return Loss (dB)	−9.82	−13.3
Coupled (dB)	−4.7	−3.44
Through (dB)	−3.15	−3.43
Isolation (dB)	−11.38	−13.3
Phase difference(deg)	90°	86.5°

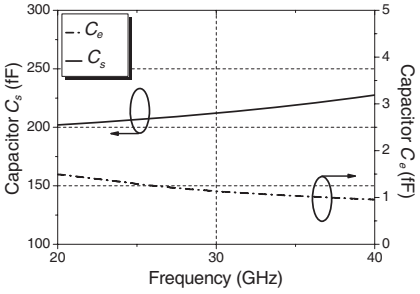

Figure 6. Extracted C_e and C_s values of the TRD coupler.

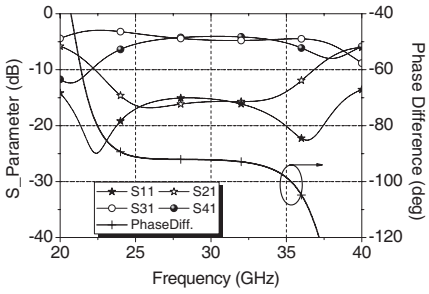

Figure 7. Full-wave EM simulated results of the coupler including the tapered leads and pads.

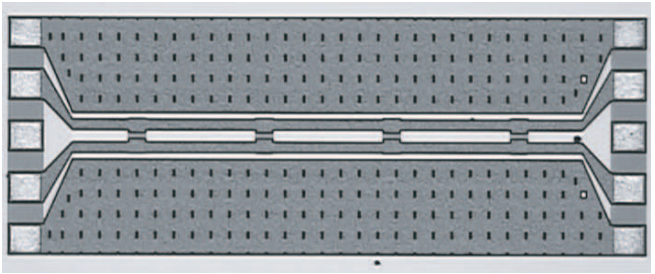

Figure 8. Photograph of the proposed coupler. The chip area including the pads is 1.1 mm × 0.46 mm.

Figure 7 shows the full-wave simulated result of the whole chip including the tapered leads and pads as shown in Fig. 8. The chip area including the pads is 1.1 mm × 0.46 mm. The measured S-parameters and phase difference are shown in Fig. 9(a). The comparison of simulated and measured phase and amplitude differences are shown

in Fig. 9(b). As it shows, even though there is mismatch between the coupler and the 50 Ω test standard, the performance is still acceptable as a 90° hybrid. The measured performance is listed in Table 3. A bandwidth from 25.05 to 32.65 GHz is achieved under the criteria of $90° \pm 5°$ phase difference and ±1 dB amplitude difference.

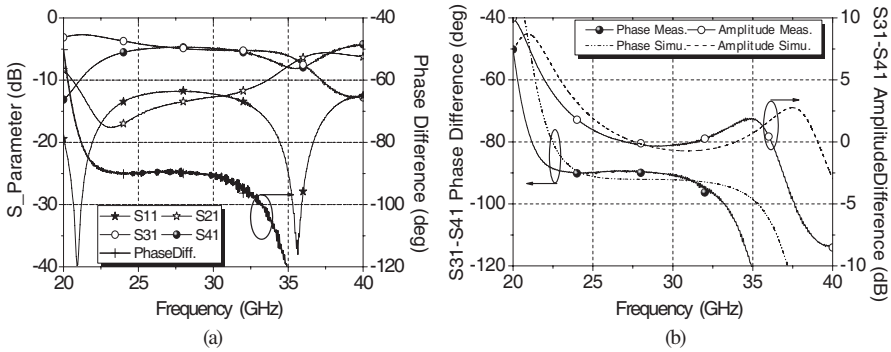

Figure 9. (a) The measured S-parameters and phase difference (b) Comparison of simulated and measured phase and amplitude differences of the proposed coupler.

Table 3. Simulated and measured results of the proposed coupler.

	Formula	Full-wave EM Simulation	Measurement
Bandwidth range (GHz)	26.8–34.05 (23.8%)	25.95–34.25 (27.6%)	25.05–32.65 (26.3%)
Phase difference $< \pm 5°$ (GHz)	24.45–36.0	23.00–34.25	21.65–32.65
Amplitude difference $< \pm 1$ dB (GHz)	26.8–34.05	25.95–35.35	25.05–33.35
Center frequency (GHz)	30.4	30.1	28.85
Isolation (S_{12})	< -16.52 dB	< -14.91 dB	< -11.16 dB
Input Return Loss (S_{11})	< -17.43 dB	< -15.03 dB	< -11.64 dB

3. DESIGNS AND IMPLEMENT OF THE QVCO CIRCUIT

By connecting the differential output ports of a cross-coupled NMOS pair to two 90° hybrids, as shown in Fig. 10, a QVCO with four signal outputs with quadrature phase difference is formed. The isolation ports are terminated with 50 Ω to further reduce the reflected power to the input ports, avoiding disturbance to the core of the resonant tank. The proposed configuration of the QVCO has several advantages. First, the required orthogonality of the output signals mainly depends on the performance of the 90° hybrids and is not influenced by the VCO itself. Therefore, the VCO can be optimized to achieve the lowest phase noise or largest output power without considering the generation of accurate quadrature signals. Second, the DC bias of the buffers of the VCO is fed from the isolation ports of the couplers. Thus, the RF chokes to the DC sources can be omitted. Due to the isolation between the input and output ports of the TRD couplers, the DC blocks to the outputs can be eliminated, too. The use of TRD couplers also results in the reduction of electrical length from typical 90° to 66.7°. All these merits of TRD couplers make it easy to fabricate all components of the QVCO on a single chip. Third, unlike Lange couplers or contra-directional couplers, the outputs of TRD couplers are on the same side, eliminating cross-over circuits

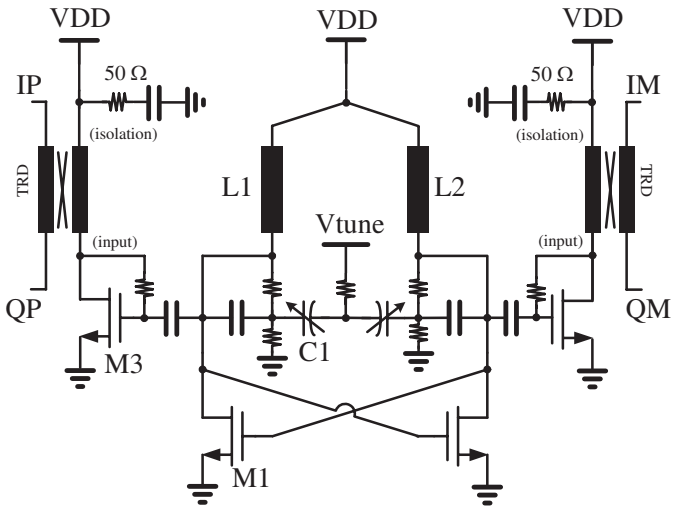

Figure 10. The schematic of the QVCO using proposed TRD couplers.

which add unpredictable losses and phase delays. Fourth, the proposed QVCO uses only two buffers comparing to four in traditional QVCOs which require one on each quadrature output path. Thus, the circuit is simpler and power consumption of the output buffers is reduced. Note that by setting the gate bias of the transistors in the output buffers to the supply voltage (VDD), stable operation against VDD variation and the required operating region can be achieved with a simple circuit configuration [22]. The main drawback of the proposed QVCO is the larger chip area to form the TRD couplers. However, its size can be reduced further by using meander-like and stacked transmission-lines to form the TRD couplers. And it may be more convenient to combine with the other circuit such as mixer.

To reach the start-up condition for oscillation at as high as 30 GHz in 0.18 μm technology, an NMOS cross-coupled pair is adopted to decrease the parasitic capacitance in the transistors. At the same transconductance, PMOS transistors exhibit more parasitic capacitance, lowering the oscillation frequency of the resonant tank. The NMOS M1 of the core circuit is composed of 18 fingers with aspect ratio 1.84 μm/0.18 μm (width/length). The NMOS M3 of the buffer circuit is composed of 64 fingers with aspect ratio 1.5 μm/0.18 μm (width/length). The accumulated-mode MOS varactor C_1 is formed by N-type diffusion and the thick oxide [21]. The thick oxide MOS varactor has a lower tuning sensitivity and a higher quality factor than the normal thin oxide varactor because it can decrease the electric field in the oxide. Thus, it can achieve a good phase noise when used to form a resonance tank. The MOS varactor is composed of 10 branch, and each branch is 0.5 μm × 2.5 μm in size. A center-taped inductor is used to implement L_1 and L_2 to minimize the chip area and to maximize the quality factor. By properly forming the inductor, the maximum quality factor of the inductor can be located at close to the operating frequency to improve the circuit performance. The simulated results reveal that the output power of the QVCO is greater than −1 dBm with a phase noise of −107 dBc/Hz at 1 MHz offset from the carrier frequency 30 GHz.

The QVCO was fabricated in CMOS 0.18 μm mixed signal process. The size of the QVCO including the testing pads is 1.39 mm × 0.68 mm. The photograph of the QVCO is shown in Fig. 11. Fig. 12 shows the measured frequency tuning range and output power level of the quadrature output ports. The frequency tuning range is from 31.9 to 32.7 GHz with tuning voltage (Vtune) varied from 0 to 1.8 Volt. The amplitude imbalance of the orthogonal signals is less than 1 dB, which is also consistent with the measured results of the TRD coupler in Fig. 9(a). Operating at the supply voltage of 1.3 V, the current

consumptions for the core circuit and each buffer of QVCO are 16.3 mA and 27 mA, respectively. The output power is −1.52 dBm. Part of the reason of this higher output power can be attributed to the TRD couplers. They enable direct supply of the bias voltage at the isolation ports without extra on-chip or off-chip RF chokes which cause extra power loss.

Direct measurement of the phase difference of the QVCO signals are very challenging at such a high frequency [23]. Since in our QVCO, the 90° phase difference required by QVCO is generated by the couplers, the performance of the couplers will determine the phase characteristics of the QVCO. From the measured results of our couplers, a phase difference of 90° ± 6° is achieved in the frequency 21.65 ∼ 32.70 GHz.

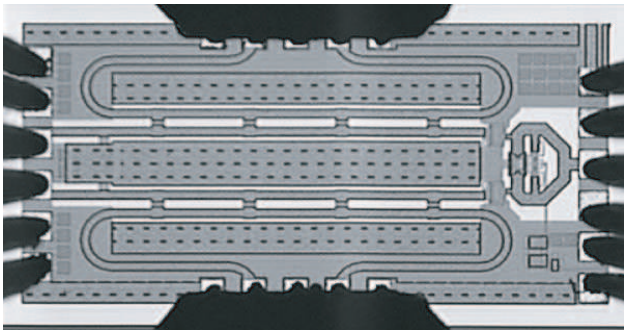

Figure 11. Photograph of the proposed QVCO circuit. The chip area is 1.39 mm × 0.68 mm.

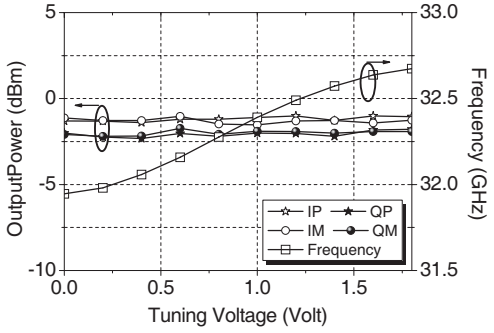

Figure 12. The measured results of the frequency range and the output power of the QVCO.

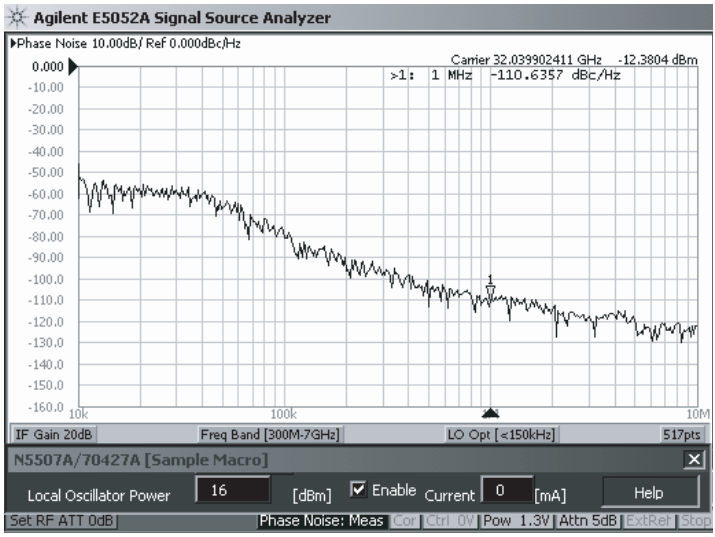

Figure 13. Measured result of the phase noise of QVCO v. s. offset frequency at zero tuning voltage.

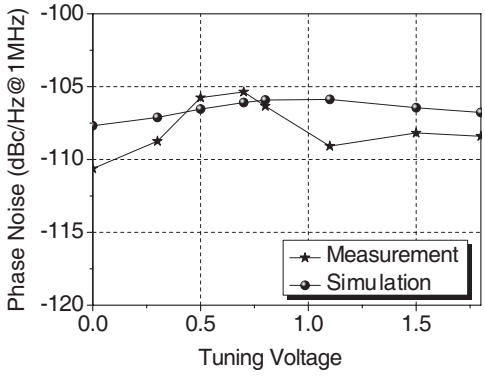

Figure 14. Simulation and measurement results of the phase noise of QVCO versus the tuning voltage.

Figure 13 shows the measured phase noise obtained by using Agilent E5052A signal source analyzer and Agilent N5507A microwave down-converter. The microwave down-converter is introduced because the measured carrier frequency has exceeded the maximum operating frequency of the signal source analyzer. A measured phase noise of $-110.6\,\mathrm{dBc/Hz}$ at 1 MHz offset from the carrier frequency 32 GHz is

achieved. A lower than −105 dBc/Hz phase noise is achieved as shown in Fig. 14 in the tuning voltage. According to the widely used Figure of Merit (FOM) for the oscillator

$$FOM = 20\log\left(f_{osc}/f_{offset}\right) - 10\log(L(f_{offset}) \cdot P_{dc}), \tag{7}$$

where $L(f_{offset})$ is the phase noise at the offset frequency from the center frequency f_{osc} and P_{dc} is the core power consumption in milliwatts. It reveals that the FOM of the QVCO is 187.5 dBc/Hz. This good result can be attributed to the simple configuration of the VCO and the adoption of the TRD couplers to generate the quadrature outputs. Finally, the comparison of the characteristics of QVCO with other reported QVCOs is shown in Table 4. Comparing to [3] and [26] which operate at similar frequency range, the proposed QVCO achieves the best output power and phase noise, but worse phase difference which can be fixed if the TRD couplers matching to 50 Ω can be implemented under the constraint of the 0.18 µm CMOS process.

Table 4. Comparison of our measurements of the proposed QVCO with other reported QVCOs.

Reference	[2]	[3]	[24]	[25]	[26]	This work
Process	InPHBT	0.25 µm SiGe BiCMOS	CMOS 0.13 µm	CMOS 0.18 µm	CMOS 0.18 µm	CMOS 0.18 µm
Including PAD Layout Size (mm^2)	0.45 × 1.25	0.7 × 0.5	0.85 × 0.6 (modulator included)	0.48 × 0.78	1.1 × 1.0 (Dual-band)	1.39 × 0.68
Operating Voltage (Volt)	3.3	5	n.a.	1	2	1.3
Core Power Consumption (mW)	122.1 ~ 171.6	140	40	5	52	21.19
Frequency (GHz)	38.0 ~ 47.8	30.6 ~ 32.6	44.8 ~ 45.8	14.8 ~ 17.6	29.5 ~ 30 /14.75 ~ 15	31.9 ~ 32.7
Output Power (dBm)	−15	−19.36	−13	−9.73	−16/−8	−1.52
Phase Noise (dBc/Hz) @1MHz	−84 ~− 86 (predicted)	− 97	−98.9	−110	−104/−112	−110.6
Amp. and Phase Error	n.a.	n.a./0.6°	0.3 dB/1.8°	n.a./ 4.5°	n.a. (quad/half-quad)	< 1.0 dB /< 6°
FOM	n.a.	n.a.	176.1	187.6	176/178	187.5

4. CONCLUSION

This work presents a new topology of the realization of CMOS QVCO by using the TRD couplers. It uses two TRD couplers, which can eliminate the use of RF chokes, to obtain the orthogonal signals. Since the phase error and amplitude imbalance of the orthogonal signals of the proposed QVCO are mainly determined by the characteristics of the coupler, the design of VCO may be optimized for better phase noise and higher output power. A 1.39 mm × 0.68 mm prototype of this QVCO operating at 30 GHz is designed and built in TSMC 0.18 μm CMOS process. An output power level of −1.52 dBm and best phase noise of −110.6 dBc/Hz are measured. A figure-of-merit of 187.5 dBc/Hz is also achieved.

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