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BALANCED MIXERS USING WIDEBAND SYMMETRIC OFFSET STACK BALUN IN 0.18 μm CMOS

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Abstract—This work proposes a symmetrical offset stack coupled lines balun and a dual balun for a single balanced mixer and a star mixer, respectively. To achieve a minimum insertion loss and a maximum bandwidth, the design formulas are derived by properly selecting the width of coupled lines and the offset width between two coupled lines. The measured results of the proposed single and dual baluns achieve the bandwidths of over 110% and 90%, and insertion losses less than 4.4 dB and 7.4 dB at 38 GHz. These two baluns occupy chip sizes of 0.07 mm^2. Two balanced diode mixers are further proposed and implemented in tsmc^{TM} 0.18-μm CMOS processes. These mixers utilize a stack balun feature wide bandwidth with very compact size. The measured results of the single balanced and star mixer achieve over 115% and 100% bandwidth for a conversion loss of < 15 dB. The isolations are better than 24 dB from 10 to 65 GHz of the single balance mixer and better than 31 dB from 20 to 65 GHz of the star mixer.

1. INTRODUCTION

Mixer is an important component in a heterodyne transceiver system because it converts signals from one frequency to another. A single balanced mixer and a star mixer use two and quad anti-parallel diodes that provide inherent rejection of the input signal at the output due to their balanced amplitude and anti-phase properties. However, these two mixers require balun to feed LO or RF signal, and the balun is the key component in mixer design.

[1] reported a resistive mixer for 60-GHz frequency range. A Lange coupler together with a $\lambda/4$ transmission line is used to generate

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the out-of-phase LO signal. [2] used a microstrip rat-race balun in single balanced diode mixer for a Ka-band satellite transponder. The measured result showed that a conversion loss is less than 9 dB at the IF frequency from 20.0 to 21.6 GHz under 6.5 dBm LO power. [3] demonstrated a V-band high isolation sub-harmonic mixer in standard 0.15-μm pHEMT process. This mixer was composed of a hairpin diplexer, an open stub, and a low-pass filter. The hairpin diplexer was used to improve the isolation between the RF and LO ports. The measured result of conversion loss was lower than 18.3 dB. LO-to-RF and 2LO-to-RF isolations were better than 23.5 and 27.5 dB over a 54–66 GHz bandwidth. The restrictions of these baluns were narrow bandwidth operation, and the chip sizes were large in low frequency design.

[4] developed a broadband mixer using three edge and broadside coupled-lines in pHEMT technology. This diode mixer achieved conversion loss better than 10 dB from 46 to 78 GHz. [5] described a single-balanced mixer using a planar coupled-lines balun in microwave and millimeter wave bands. The best up-conversion loss was 8 dB with an LO-RF isolation better than 30 dB. A 16-46 GHz mixer using a broadside-coupled balun fabricated in standard CMOS process achieved a bandwidth from 16 to 46 GHz with a conversion loss ranging from 13 ± 1.5 dB and a compact chip size of 0.24 mm^2 [6]. [7] employed an edge-coupled transmission line Marchand balun to feed the LO and RF ports of a ring-type W-band DBM. [8] designed a doubly balanced mixer using two novel configurations of dual baluns in 0.15 μm GaAs pHEMT process. The conversion loss was 6.6 to 10.6 dB within an RF bandwidth from 24 to 40 GHz. The measured LO-to-RF, LO-to-IF and RF-to-IF isolations were higher than 20, 20 and 22 dB from 22 to 40 GHz, respectively. However, the available design parameters of these baluns were limited by their width and space of the edge coupled lines or the width and thickness of the broadside coupled lines which performance was thus restricted.

[9] utilized a lumped frequency diplexer and a low-pass filter for a 16–31 GHz sub-harmonic mixer, whose chip area was 0.57 mm^2, in 0.15 μm GaAs pHEMT process. The lumped frequency diplexer consisted of a low-pass and a high-pass network to reduce the chip size and improved the isolation between the RF and LO ports. [10] presented an L-C lumped element balun to implement an MMIC star mixer, whose conversion loss less than 10 dB was from 1.5 to 5.2 GHz. The lumped baluns were narrow band operation.

[11] presented a broadband, high isolations and a compact chip area doubly balanced ring mixer in 0.15 μm GaAs pHEMT process. The spiral balun with low-pass filter was used to extract IF signals

and maintained balun performance simultaneously. The measured conversion loss was lower than 12.4 dB. The LO-IF, RF-IF and LO-RF isolations were better than 43.2, 32 and 26.9 dB from 11 to 40 GHz, respectively. Several dual balun designs such as double spiral transformer, trifilar transformer and 3-D transformer dual balun [12] were developed for the performance of good amplitude/phase balance, low loss and wide bandwidth. The restrictions of these baluns are the magnetic flux leakage and the parasitic capacitance between the windings, which limited their high frequency response.

To overcome the aforementioned limitations, the authors propose a single balun and a dual balun using symmetrical offset stack couple lines structure [13]. The stacked and meandered line topologies are used in balun design, not only saving the chip area but also having tight coupling characteristic (i.e., wideband performance). Moreover, the offset width of the stack coupled line offers additional design freedom to optimize the balun performance. Then a single balanced mixer and a star mixer utilizing the adopted balun were fabricated in standard 0.18-μm CMOS technology, which achieved low conversion loss and wide bandwidth performance.

2. CIRCUIT DESIGN

This paper begins with an introduction of symmetrical offset stack coupled line balun and dual balun. Using these baluns, two balanced mixers are developed to achieve the performance of wideband, low conversion loss, high isolation and low LO power in 0.18-μm CMOS process.

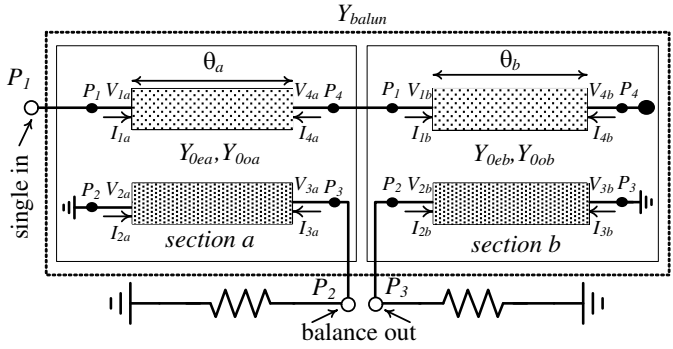


Figure 1. Block diagram of a Marchand Balun with two identical coupled-line sections.

2.1. Single Balun Design

Figure 1 shows the schematic diagram of a Marchand balun with two identical coupled-line sections (sections a and b). The even/odd mode characteristic admittances of the two sections are denoted as Y_{0ea}/Y_{0oa} and Y_{0eb}/Y_{0ob}. The electrical lengths of section a and b are θ_a and θ_b. The voltage and current of each port in sections a and b are denoted as V_{1a}, V_{2a}, V_{3a}, V_{4a}, I_{1a}, I_{2a}, I_{3a}, I_{4a} and V_{1b}, V_{2b}, V_{3b}, V_{4b}, I_{1b}, I_{2b}, I_{3b}, I_{4b}, respectively. When the coupled-line sections are replaced by their admittance matrix, the corresponding Y-parameters matrix of the coupled line structure, in terms of the Y_{0e} and Y_{0o} are given by (1). (let $Y_{0e} = Y_{0ea} = Y_{0eb}$, $Y_{0o} = Y_{0oa} = Y_{0ob}$ and $\theta = \theta_a = \theta_b$)

$$Y = N \begin{bmatrix} \cot\theta & M\cot\theta & -M\csc\theta & -\csc\theta \\ M\cot\theta & \cot\theta & -\csc\theta & -M\csc\theta \\ -M\csc\theta & -\csc\theta & \cot\theta & M\cot\theta \\ -\csc\theta & -M\csc\theta & M\cot\theta & \cot\theta \end{bmatrix} \tag{1}$$

where $N = -j(Y_{0e} + Y_{0o})/2$ and $M = (Y_{0o} - Y_{0e})/(Y_{0o} + Y_{0e})$.

The two connected coupled-line networks in Fig. 1 can be viewed as a three-port network. The insertion loss of the balun can be expressed as (2).

$$S_{21} = -S_{31} = 2Y_0C(Y_0 + B + D)/\Delta \tag{2}$$

where

$$A = N(X\cot\theta + 1)/(X + \cot\theta) \tag{2a}$$

$$B = N\cot\theta\left(X + \cot\theta - M^2\cot\theta\right)/(X + \cot\theta) \tag{2b}$$

$$C = NM\csc\theta/(X + \cot\theta) \tag{2c}$$

$$D = -NM^2X\cot\theta/(X + \cot\theta) \tag{2d}$$

$$X = \cot\theta - \csc\theta\sec\theta \tag{2e}$$

$$\Delta = (Y_0 + B + D)\left((Y_0 + A)(Y_0 + B + D) - 2C^2\right) \tag{2f}$$

S_{21} and S_{31} are the function of M and θ with the same magnitude and 180° out of phase.

Figure 2(a) shows the 3-D view of the proposed stack balun. The tsmc$^{\text{TM}}$ 1p6m CMOS technology provides six metallization layers. The balun structure is formed by two metal layers (M_6/M_4). The width of upper and lower transmission lines is W, and the offset width of two coupler is S. The height between M_6 and M_4 is 2 μm and 10 μm between M_4 and top of substrate. The thickness of substrate is 300 μm. The input signal is fed to the metal layer M_6, which has thick metal up to 2.3 μm that provides low resistance to obtain a low loss transmission line. The balanced outputs are taken out from the inner metal M_4 with

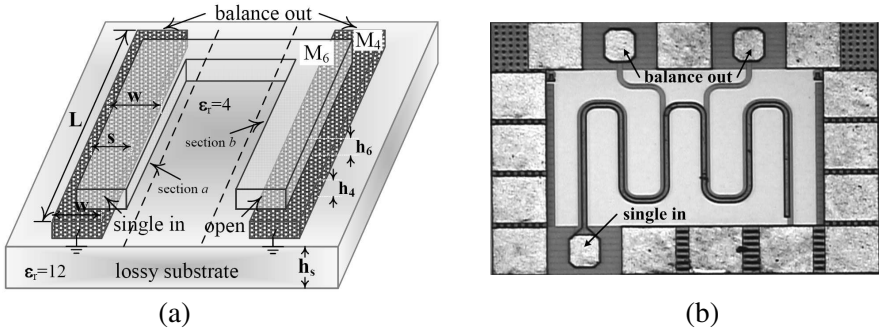


Figure 2. (a) 3-D view. (b) Chip photograph of the symmetrical offset stack balun.

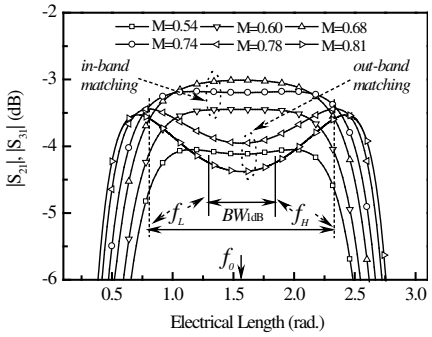


Figure 3. The S_{21} and S_{31} of the symmetric offset stack Marchand balun.

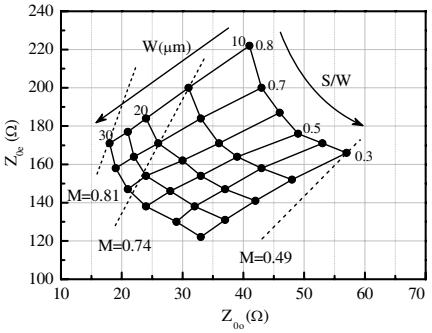


Figure 4. Extracted Z_{0e} and Z_{0o} for symmetric offset stack coupled lines with different transmission lines width (W) and offset ratio (S/W).

a 0.56 μm thickness. The balun with two $\lambda_g/4$ symmetrical coupled-line sections (sections a and b) is shown in Fig. 2(a).

Figure 3 shows the insertion loss frequency response between BW and M of the Marchand balun. When $M \leqq 0.54$ or $M \geqq 0.75$, the insertion loss at center frequency (f_0) increases, and the lowest insertion loss will occur at both high and low frequencies. We call these cases out-band matching. The $\mathrm{BW}_{-1\,\mathrm{dB}}$ is defined as $f_H - f_L$ at $IL(f_0) + 1\,\mathrm{dB}$. When $0.54 \leqq M \leqq 0.75$, the in-band matching cases exhibit the lowest IL at center frequency, and the defined 1-dB bandwidth of IL ($BW_{-1\,\mathrm{dB}}$) is $f_H - f_L$. The flat frequency response occurs at $M = 0.74$, as can be observed in Fig. 3.

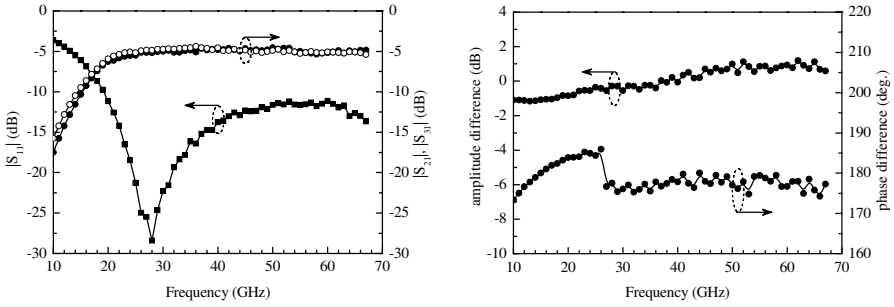


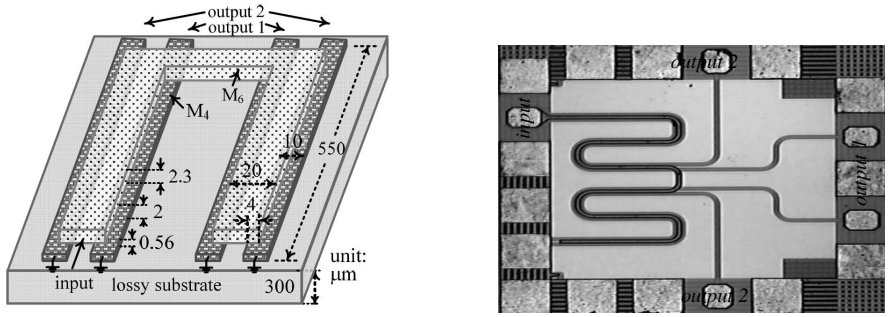
Figure 5. Measured results of the balun. (a) Insertion and return losses. (b) Magnitude and phase difference.

Figure 4 indicates the extracted Z_{0e} and Z_{0o} for different W and S/W by full-wave electromagnetic simulator, HFSS^{TM}. If W is larger, the Z_{0e} and Z_{0o} become smaller. If S/W is smaller, the Z_{0e} becomes smaller, thus increasing the Z_{0o} impedance. Since the relationship between Z_{0e} (Z_{0o}) and S/W has been founded, we can use M to find the desired transmissions width W and offset ratio (S/W). In balanced mixers applications, $W = 20\,\mu\text{m}$ and $S/W = 0.7$ (i.e., $M = 0.74$, $Z_{0o} = 26\,\Omega$ and $Z_{0e} = 170\,\Omega$) are chosen to be close to $50\,\Omega$ to achieve the maximum bandwidth, low IL and minimum imbalance of the balun.

The proposed symmetrical offset stack balun is fabricated by using $0.18\,\mu\text{m}$ CMOS technology. Fig. 2(b) shows the chip photograph, whose size is $0.07\,\text{mm}^2$, excluding pads. The S-parameters from 10 to 67 GHz are measured using an Agilent N4421BH67 four-port network analyzer. Fig. 5 shows the measured results of the proposed symmetrical offset stack balun. The measured return loss and insertion loss are better than 10 dB and less than 6.5 dB from 19 to 67 GHz, respectively. The measured amplitude difference is less than ± 1 dB, and the phase difference is less than $180 \pm 4^\circ$ from 10 to 67 GHz. Because the field is mostly concentrated between two stack coupled lines, the minimum insertion loss is 4.4 dB at 38 GHz (3 dB for an ideal balun). This millimeter-wave balun exhibits low loss, broadband characteristics (more than 110%) and is compact in size.

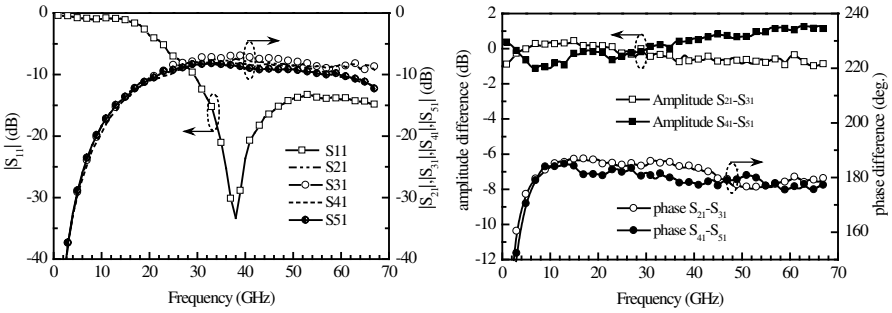
2.2. Dual Balun Design

Figure 6(a) shows the schematic drawing of the proposed dual balun, formed by two parallel single Marchand baluns. The structure of dual balun is formed with two metal layers (M_6/M_4). The input signal is fed



(a) (b)

Figure 6. (a) 3-D view. (b) Chip photograph of the proposed dual balun.



(a) (b)

Figure 7. Measured results of the dual balun. (a) Insertion and return losses. (b) Magnitude and phase difference.

to the metal M_6, which has thick metal up to 2.3 μm that provides low resistance to obtain a low loss couple line. The two pairs of balanced outputs are taken out from the metal M_4 with a 0.56 μm thickness. The width of the upper and lower coupled lines are 20 and 10 μm, respectively, and the offset width of coupled line is 4 μm. The height between M_6 and M_4 is 2 μm and 10 μm between M_4 and top of the substrate. The thickness of the substrate is 300 μm.

The design method of the dual balun is described as below. The single balun was designed firstly. The dimension of the coupled lines is selected as $W = 10\,\mu m$ and $S/W = 0.4$ with an electrical length of $\lambda_g/4$, which has a physical length of 550-μm at the center frequency of 38 GHz. As can be observed in Fig. 4, the odd-mode and even-

mode impedances of single balun are 57 Ω and 155 Ω, respectively. The impedance of the single balun can be calculated as 94 Ω. By paralleling two single baluns, the input impedance Z_0 of the dual balun is 47 Ω, which provides a good match at RF/LO ports.

Figure 6(b) shows the chip photo of dual balun whose size is 0.07 mm^2. The measured results are shown in Fig. 7. The insertion loss from 22 to 58 GHz is lower than 10 dB, and the return loss is better than 10 dB from 30 to 67 GHz. A ±1-dB amplitude difference and a $180 \pm 5^\circ$ phase imbalance are obtained from 11 to 50 GHz.

2.3. Single Balanced and Star Mixers Design

2.3.1. Single Balanced Mixer

Figure 8(a) shows the schematic of the single balanced mixer. This mixer consists of a single balun, two GD-connected diodes, and a low pass filter. The impedance of the diode ($Z_d = 54\,\Omega$) can be calculated according to $Z_d = (2Z_{0o})^2/Z_s$, where Z_S (50 Ω) is the source impedance, and Z_{0o} (26 Ω) is the balun odd-mode impedance. Four fingers with total width 44-μm NMOS transistors are selected as the mixing device. The impedance level is 54 Ω from 10 to 65 GHz, under an 11-dBm LO power pumped through the balun. The optimized odd impedance of diode is selected to match for the adopted balun directly to eliminate the matching circuits between the balun and the diodes, and thus results in wide bandwidth and compact size. The LO signal leaking through the diode capacitance is canceled at the RF/IF ports due to their anti-phase LO relationship. At RF port, a small series capacitor is employed as a high-pass filter to provide IF-to-RF isolation. At IF port, a low-pass filter consisting of an inductor and a

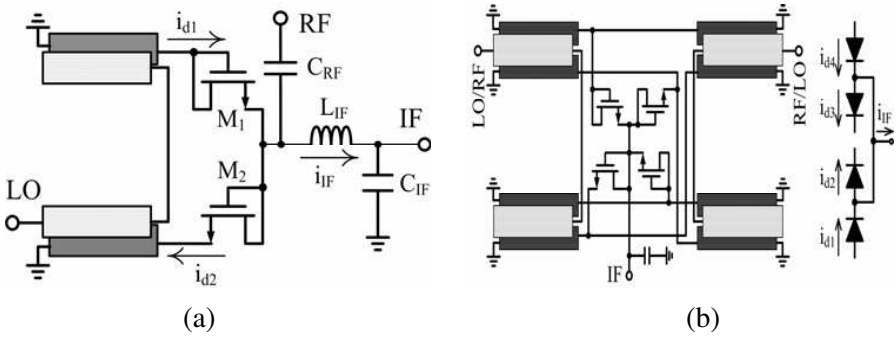


Figure 8. Circuit schematic diagram. (a) Single balanced mixer. (b) Star mixer.

shunt capacitor is used to increase LO-to-IF and RF-to-IF isolations. The current flow of the mixer is shown in Fig. 8(a), and the resulting IF output current is represented in $i_{IF} = ((-1)^m - 1)i_{d2}$, where m is the order of RF harmonics. For the mixer operation, while $m = 1$, and i_{IF} is two times of i_{d2}.

2.3.2. Star Mixer

Figure 8(b) shows that the schematic of star mixer consists of a pair of dual baluns for LO and RF signals and a quad diode for mixer core. Using the ADS^{TM} MOMENTUM EM simulator, the calculated Z_{0o} of dual balun is 25 Ω. The impedance of star quad diode ($Z_d = 50\,\Omega$) can be calculated according to $Z_d = (2Z_{0o})^2/Z_s$, where Z_S (50 Ω) is the source impedance, and Z_d is the impedance of an individual diode. In our design, the mixer diode was implemented using the GD-connected N-MOSFET. The finger and width/length of each diode was selected as 16 and 64/0.18 µm. The impedance level is 50 Ω from 20 to 60 GHz under an 11-dBm LO power pumped through the dual balun. The IF signal is directly taken out from center of the diode quad. Fig. 8(b) shows the circuit schematic diagram and current flow of the star diode mixer, and the resulting IF output current represents in $i_{IF} = ((-1)^m - 1)((-1)^n - 1)i_{d1}$, where m and n are the order of LO and RF harmonics, respectively. For the star mixer operation, while m and n are even the i_{IF} equals zero, whereas m and n are odd the i_{IF} is four times of i_{d1}. Therefore, it obtains better suppression of even-order spurious signals at the IF output.

3. MEASURED RESULTS

Figure 9(a) shows the chip photograph of the single balanced mixer, whose size is 0.24 mm^2. Fig. 10(a) shows the measured conversion loss of IF and RF bandwidth at −15-dBm RF power and an 11-dBm LO power. The measured IF conversion loss is less than 15 dB from 0.1 to 3.1 GHz. The measured conversion loss is lower than 15 dB from 14 to 52 GHz which is correspondent with an RF bandwidth of 115%. The minimum conversion loss is 10.5 dB at the RF frequency of 20 GHz. The measured isolations are shown in Fig. 10(b). The LO-RF, LO-IF and RF-IF isolations exceed 24 dB, 41 dB and 34 dB, respectively, with the LO and the RF frequencies varied from 10 to 65 GHz, respectively.

Table 1 summarizes the performance of the recently published millimeter-wave single balanced mixers. The proposed mixer achieves a wide bandwidth of over 115%, which is the widest documented bandwidth relative to the cited MMIC designs. Work [2] has the lowest

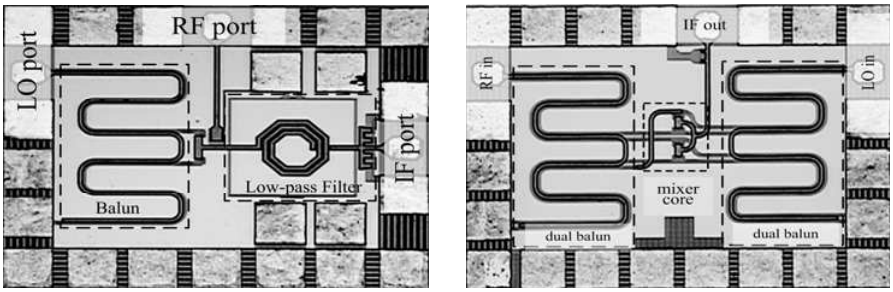


Figure 9. Chip photograph. (a) Single balanced mixer. (b) Star mixer.

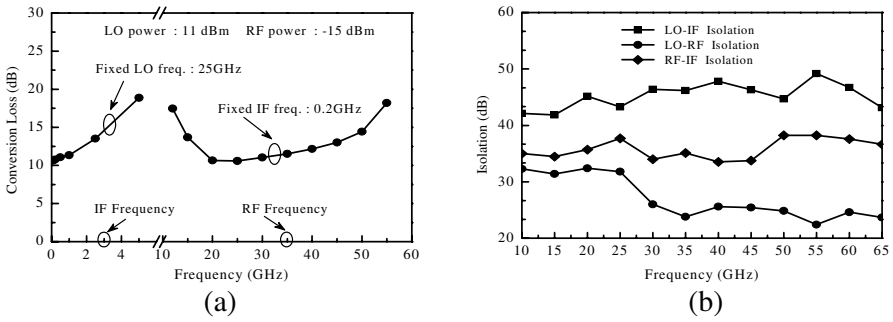


Figure 10. Measured results of the single balanced mixer. (a) IF and RF conversion losses. (b) Port to port isolations.

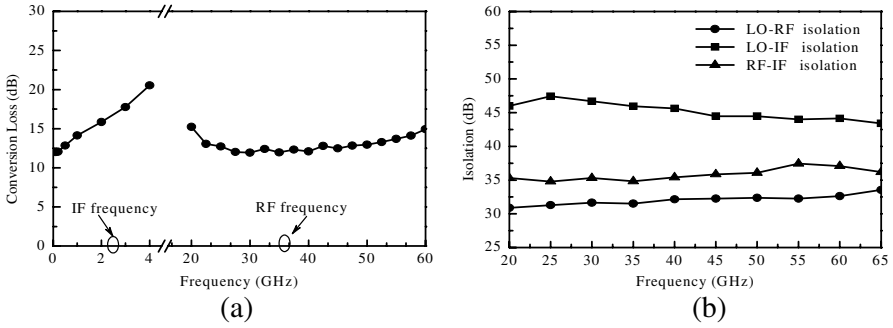


Figure 11. Measured results of the star mixer. (a) IF and RF conversion losses. (b) Port to port isolations.

Table 1. Performance benchmark of the recently published single balanced mixers.

References	[1]	[2]	[3]	[4]	[5]	This Work
Process	0.25 μm pHEMT	Package	0.15 μm pHEMT	0.25 μm pHEMT	0.18 μm CMOS	0.18 μm CMOS
RF Freq. (GHz)	57–67	29.8–31.4	46–78	15–22	12–22.5	14–52
B.W. (%)	16.1%	5.2%	51.6%	37.8%	61%	115%
Conv. Loss (dB)	11.5	8–9	7–10	8.3–12	< 10	10.5–15
LO Power (dBm)	8	6.5	12.5	15	11	11
Isolation (dB)						
LO-RF	34	N/A	20	30	25	24
LO-IF	N/A	N/A	N/A	40	37	41
Chip Area (mm^2)	3	1350	0.3	32.5	0.24	0.24

conversion loss and LO power. However, it operates at low frequency band, and the chip size is very large. Compared with the p-HEMT mixer designs, this work obtains better wide bandwidth, and compact size. Compared with the same CMOS mixer designs [5], our proposed mixer has better performance of bandwidth.

Figure 9(b) shows the chip photograph of the star mixer, whose size is $0.6 \times 0.4\,mm^2$. Fig. 11(a) presents the measured conversion loss of the star mixer. This mixer with the symmetric offset dual balun has a bandwidth of 100% and a conversion loss of less than 15 dB from 20 to 60 GHz. The minimum conversion loss is 11 dB under 11-dBm LO power at 30 GHz and a fixed IF frequency of 0.2 GHz. The characteristic of the IF bandwidth at the 11-dBm LO power and -15-dBm RF power is less than 15 dB at IF frequencies from 0.1 to 1.5 GHz as shown in Fig. 11(a). The measured port-to-port isolations of the mixer are shown in Fig. 11(b). The measured LO to RF and LO to IF isolations are better than 31 dB and 44 dB at RF frequencies from 20 to 65 GHz. The RF-IF isolation is better than 35 dB, and the single balanced resistive mixer provides good port-to-port isolations.

Table 2 compares the proposed star mixer with the cited millimeter-wave double balanced mixers. The mixers in [9, 10] achieve conversion losses of less than 12.4 dB and bandwidths of

Table 2. Performance bench mark of the double balanced mixer.

References	[5]	[9]	[10]	[11]	[12]	This Work
Process	0.18 µm CMOS	0.15 µm pHEMT	GaAs	0.13 µm CMOS	0.15 µm pHEMT	0.18 µm CMOS
RF Freq. (GHz)	25–56	11–40	1.5–5.2	25–45	28–40	20–60
B.W. (%)	76.5%	114%	110%	57.1%	35.3%	100%
Conv. Loss (dB)	15	7.2–12.4	8.5–10	8–14	6.6–10.6	11–15
LO Power (dBm)	11	13	17	6	13	11
Isolation (dB)						
LO-RF	35	26.9	15	30	20	31
LO-IF	50	43.2	15	40	31	44
RF-IF	30	32	NA	30	23	35
Chip Area (mm^2)	0.34	0.72	0.64	0.34	1.53	0.24

over 110%. However, they need high LO power and occupy large die size. Compared with the same CMOS process, such as [5, 11], our proposed star mixer has better bandwidth performance with comparable conversion loss and port-to-port isolations.

4. CONCLUSION

A single balanced mixer and a star diode mixer utilizing the inherent 3-D multilayer structure wideband symmetrical offset stack baluns in CMOS process have been proposed. By controlling the even/odd mode impedances, the single balun and dual balun have been demonstrated in a minimum insertion loss of 4.4 dB at 35 GHz and 7.4 dB at 38 GHz, respectively. The measured amplitude/phase imbalances of single and dual baluns are 1-dB/4° and 1-dB/5°, respectively. The proposed single balanced mixer achieves a bandwidth of 115%, a conversion loss lower than 15 dB, a port to port isolation higher than 24 dB, and an IF bandwidth of 3.1 GHz, respectively. The measured conversion loss, port to port isolations and IF bandwidth of star mixer are lower than 15 dB, higher than 31 dB, and 1.5 GHz, respectively.

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